

## SIMPLE ANALYTICAL MODELING OF GaAs MESFET NONLINEAR BEHAVIOR

Takahisa Kawai\*, Student Member, IEEE  
and

F.J. Rosenbaum, Fellow, IEEE

Department of Electrical Engineering  
Washington University

(\* Author is now employed by Fujitsu Ltd.)

## ABSTRACT

A simple resistive model for the GaAs MESFET which accounts for many of its nonlinear properties is proposed. A new DC characterization approach is suggested and used to predict the performance of a single-stage feedback amplifier. Good agreement is obtained between theory and experiment.

## INTRODUCTION

The nonlinear behavior of GaAs MESFETs in the large signal region has been modeled extensively (1-4) and has been implemented in microwave CAD programs such as microwave SPICE.(5) These models include descriptions of mechanisms for the nonlinearities and the performance of the device is analyzed in conjunction with the linear parasitic and matching circuitry. Prediction of nonlinear circuit performance is now possible to a satisfactory degree with these sometimes complicated models. However, no work has yet clarified the contribution of the intrinsic FET resistive nonlinearity to total performance. The intent of this work is to illustrate the characteristic of the intrinsic nonlinearity exclusively, by employing only the FET I-V characteristic. The analysis of the nonlinearity is performed with a constant and parabolic transconductance model. The harmonic content of the output is analyzed and is shown to effectively represent details of the FETs operating behavior.

The second goal is to verify to what extent the resistive model can be used to simulate device performance. It is shown that the RF simulation based on Curtice-Ettenberg DC characterization (4) can be improved with a new approach.

## ANALYSIS OF NONLINEARITY BY SIMPLIFIED TRANSCONDUCTANCE MODELS

FET nonlinearities may be resistive or reactive, e.g. nonlinear gate capacitance variations with gate voltage. The

transconductance characteristic is considered to be the major nonlinear source in FET operation. In general, the drain current-gate voltage transfer curve has a square law behavior in gate voltage; pinch-off gives a lower limit and gate-source Schottky conduction gives an upper limit to the drain-source current swing. The limiting characteristic can result in gain-saturation and heavy output waveform distortion. The effect of nonlinearity due to the limiting has been numerically simulated with a constant limiting characteristic. First, a constant transconductance model (Fig. 1 (a)) was used in the simulation to exclude the nonlinear effect of the square-law characteristic. The combination of the constant limiting and square law transfer characteristic (Fig. 1 (b)) is used in the second simulation.

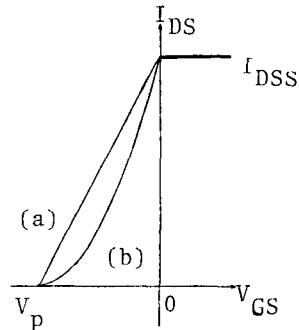


Figure 1 Simplified Transfer Characteristics  
(a) Linear (b) Parabolic

MESFET performance is simulated by applying a sinusoidal voltage to the assumed transconductance expression. The harmonic content of the output current in a resistive load is analyzed with the dependence of the gate-source DC bias. The resistive model does not take the frequency dependency into account.

A result of simulation with the square law model is shown in Figure 2. Because of the square-law characteristic, the second harmonic is present even at low drive levels. The bias dependency of the fundamental output component is shown in Figure 3. Gain compression and expansion is clearly seen even with this simple

model. Hard clipping can be obtained by center gate-source biasing. The constant transconductance model does not generate a second harmonic component and exhibits no gain expansion or compression.

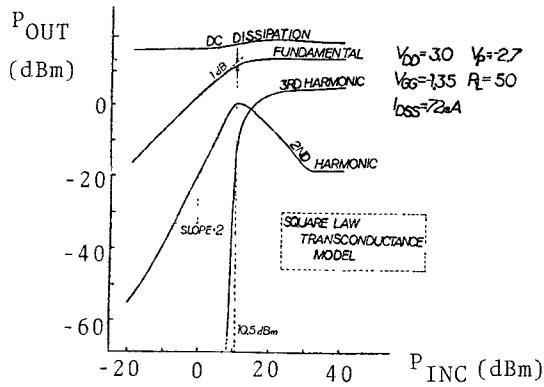


Figure 2 Harmonic Analysis with the Simplified Model

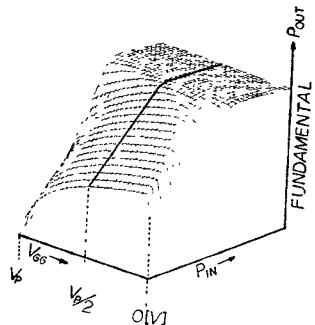


Figure 3 Gate Bias Dependency of Fundamental Output Component

#### A NEW I-V MODEL

With the square-law transfer characteristic the limiting performance near pinch-off has a critical effects on the FET nonlinear behavior. Our studies have shown that both the shape of the transconductance and the value of  $V_p$  depends on the drain-source voltage  $V_{DS}$ . For example, see Fig. 4 (a,b). These figures show that the drain current increases near pinch-off as  $V_{DS}$  increases. Also,  $V_p$  becomes more negative. Note that the current at  $V_{GS}=0.0$  V converges toward one point. This is even more evident if the leakage current is subtracted. (The flat lines near the pinch-off in Figure 4 (b) are due to instrumentation error.)

In order to obtain precise predictions we have found it necessary to examine other models for the FET DC characteristics. The results are then used to develop our I-V model. Curtice's model is widely used and gives good results for some useful ranges of the variables. His analytic expression used to express nonlinearity is

$$I_{DS} = (A_0 + A_1 V_{GS} + A_2 V_{GS}^2 + A_3 V_{GS}^3) \tanh \alpha V_{DS} \quad (1)$$

where  $A_0$ ,  $A_1$ ,  $A_2$ ,  $A_3$ , and  $\alpha$  are coefficients to be determined. The first factor describes the influence of  $V_{GS}$  while the second introduces the effect of  $V_{DS}$ . However, this factor is not particularly valid for low  $V_{DS}$  values. Figure 4 also shows that the shape of the transfer characteristic changes with  $V_{DS}$ . This effect is not included in the Curtice-Ettenberg model. (4)

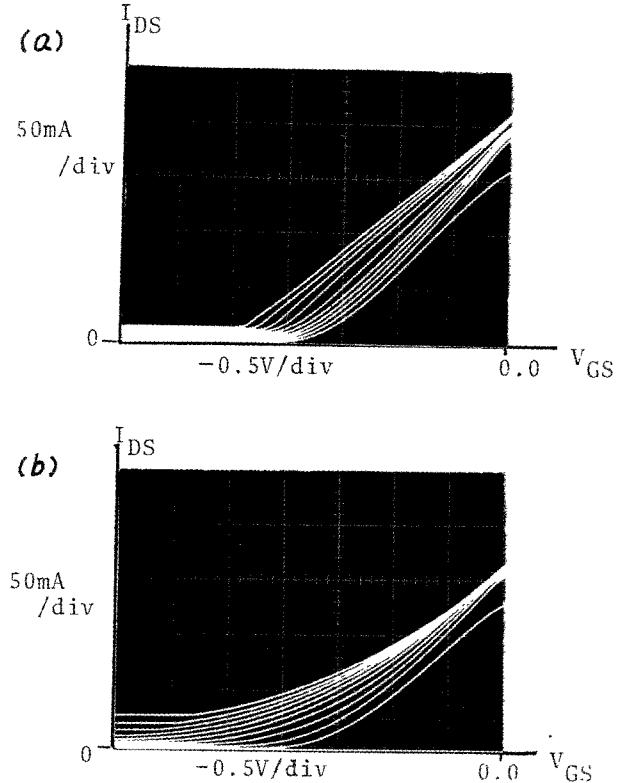


Figure 4 Transconductance Curves of  
 (a) Mitsubishi 1801 GaAs FET  
 (b) Microwave Technology FP-1  
 (The parameter is  $V_{DS}$ ,  $V_{DS}=0 - 10$  V with 1 V step)

In order to obtain more flexibility in modeling the transfer characteristics, a new DC characterization method was developed.

Figure 5 shows typical static I-V curves for a Mitsubishi 1801 FET. These curves can be represented by two functions, a polynomial function for low  $V_{DS}$  ( $0 \leq V_{DS} \leq V_k$ ) and a linear one for  $V_{DS} > V_k$ . Here  $V_k$  is the value of  $V_{DS}$  at the knee of the curve. The expression for the polynomial region is given by

$$I_{DSP}(V_{GS}, V_{DS}) = \sum_{m=0}^{3,3} A_{mn} V_{GS}^m V_{DS}^n \quad (2)$$

where  $A_{mn}$  are coefficients to be determined. Above the  $V_k$ , the linear region is defined by

$$I_{DSL}(V_{GS}, V_{DS}) = b(V_{DS} - V_k) + I_K(V_{GS})$$

$$b = \sum_{n=0}^2 b_n V_{GS}^n \quad (3)$$

where  $b$  is the slope after the current saturates, and  $I_K$  is the current at the knee voltage as a function of  $V_{GS}$  given by Eq.(2). Note the slope  $b$  is a parabolic function of  $V_{GS}$ .

In view of the fact that the pinch-off voltage is dependent on  $V_{DS}$ , this effect is taken into account with the following formula,

$$V_{p\text{dynamic}} = \frac{V_{p\text{max}} - V_{p\text{min}}}{V_{DS\text{max}} - V_k} (V_{DS} - V_k) + V_{p\text{min}} \quad (4)$$

where  $V_{DS\text{max}}$  is the maximum drain-source voltage of the I-V curve,  $V_k$  is the knee voltage,  $V_{p\text{min}}$  is the minimum pinch-off voltage, and  $V_{p\text{max}}$  is the maximum pinch-off voltage. It is assumed that the pinch-off voltage changes linearly from  $V_{p\text{min}}$  to  $V_{p\text{max}}$  between  $V_k$  and  $V_{DS\text{max}}$  along  $V_{DS}$ .

The coefficients in Eqs.(3) and (4) can be determined with the least square approach.

Figure 5 depicts the comparison of the results with Curtice's model and the polynomial-linear one for the FET in Figure 4 (a). Significant improvement of fitting is observed in both regions. The error around the knee is important because the path of load line often intersects this region. Load lines with different resistance are also drawn on Figure 5.

From the transconductance point of view, the convergence seen in Figure 4 can now be simulated with this function and is shown in Figure 6.

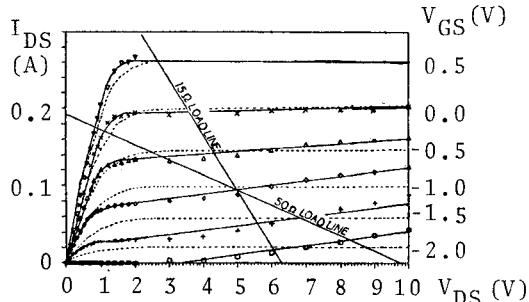


Figure 5 I-V Characteristic Simulated by Curtice-Ettenberg Model and Polynomial-Linear Function Model  
 $\times \diamond \triangle \square$  Measured  
---- Curtice-Ettenberg Model  
—— Polynomial-Linear Model

#### RF SIMULATION

RF operation of a feed-back amplifier was simulated using both the Curtice-

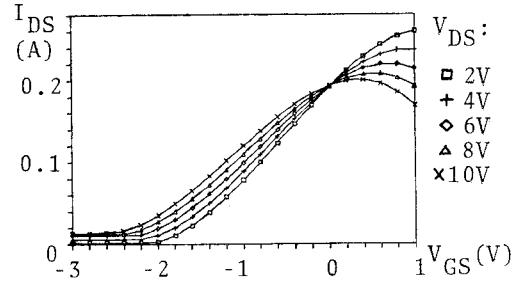


Figure 6 Transfer Curves Simulated by Polynomial-Linear Function Model

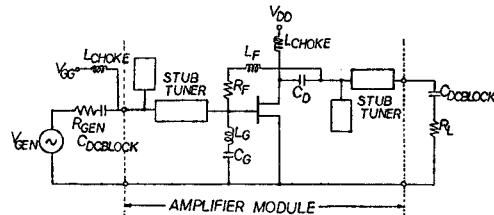


Figure 7 Circuit Diagram Used in the Experiment

Ettenberg model and the proposed one. The amplifier module used the GaAs MESFET with the I-V curves shown in Figure 4 (a). Its equivalent circuit is shown in Figure 7. A source frequency of 2 GHz was used in the experiment. The reactive elements were replaced with resistive components which give the best simulation results. This was done to simplify the analysis and to avoid the solution of circuit differential equations. Gate-source Schottky diode conduction and avalanche breakdown of drain-source are taken into account in the simulations.

Fig. 8 (a,b) compares the experimental results, the Curtice-Ettenberg model (C-E Model), and the polynomial-linear one (P-L Model) in class A operation. Even with these simple resistive models, the 1 dB compression point and the DC dissipation can be predicted with reasonable accuracy. The second harmonic component exhibits sharp notches in both simulations while the experimental results does not. We can deduce that the experimental saturated waveform is non-symmetric. The C-E model gives better result for the second harmonic in the small signal region, to within 2 dB of measured data. The P-L model shows better agreement in third harmonic with the small signal region. Neither model describes the behavior in hard limiting.

Class B operation is plotted in Fig.9 (a,b). Except for the third harmonic component, P-L model gives better agreement.

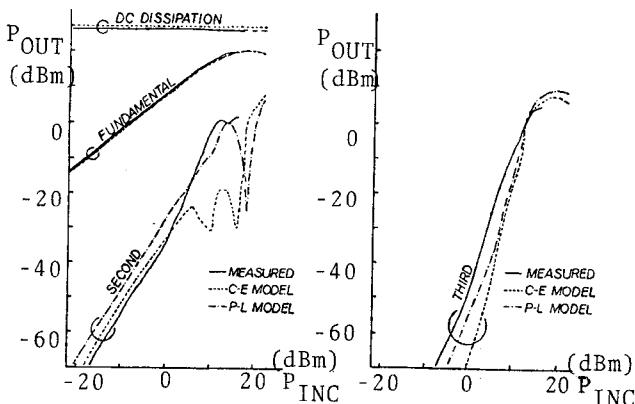


Figure 8 RF Simulation Results in Class A Operation (a) DC DISSIPATION, FUNDAMENTAL, SECOND HARMONIC (b) THIRD HARMONIC

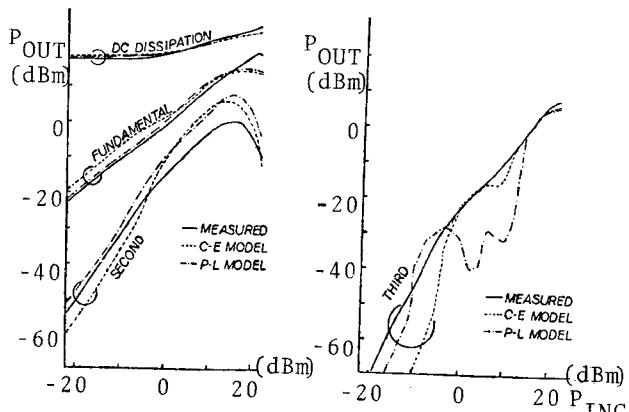


Figure 9 RF Simulation Results in Class B Operation (a) DC DISSIPATION, FUNDAMENTAL, SECOND HARMONIC (b) THIRD HARMONIC

characterization, did not necessarily predict better RF performance. It is assumed that difference between the simulated results and the measured one are due to reactive nonlinearities not considered in this study.

#### ACKNOWLEDGEMENT

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#### CONCLUSIONS

The modeling obtained by the use of the transconductance gives a simple means of understanding many of the aspects of FET nonlinear behavior. Simulations with a parabolic transfer function show that gain expansion and compression depend on the linear part of the transconductance characteristic. Hard limiting is best obtained with symmetric biasing, centered between pinch-off and forward conduction of the gate-source diode.

DC characterization error associated with the C-E model was improved by the P-L model. Simulations performed with these models give reasonably good predictions of DC dissipation, small signal gain, 1 dB compression point, saturated power and the small signal harmonics behavior. The P-L model, which gives a more accurate DC